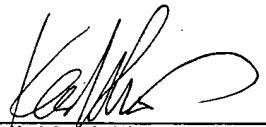
Claim 1 contains many constituent inventive elements, one of which is the step of forming an anisotropic conductive layer on a target surface such that the plurality of terminal forming areas which have been specified on this target surface will be spanned. To the best of the present inventors' knowledge, this has never been done. The prior art technology taught preparing such an anisotropic conductive layer for each of the "terminal forming areas" each corresponding to one of the electronic devices to be mounted to the target surface. According to the present invention, by contrast, a plurality of semiconductor devices are surface-mounted on one single sheet of anisotropic conductive material. This can best be seen in Fig. 4 wherein an anisotropic conductive layer 5 is shown as having been formed in a convenient shape so as to cover a plurality of terminal forming areas where a plurality of semiconductor devices D1, D2 and D3 are to be mounted.

Matsui does not disclose or hint at using such a particularly shaped anisotropic conductive layer for surface-mounting many devices at their respective "terminal forming areas". As stated at the beginning, since Matsui fails to disclose or hint at this important inventive element which limits the scope of claim 1, it should be concluded that Matsui cannot predicate the rejection of claim 1 and any claim dependent therefrom on the anticipation ground.

Respectfully submitted,



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